CLAIMS

1. (Canceled)

2. (Previously presented) The display controller of claim 7 where the internal vertical refresh rate is provided to the display for displaying the image data at the internal vertical refresh rate.

3. (Previously presented) The display controller of claim 7 where the failsafe enable circuit generates the failsafe enable signal responsive to a comparison of the input and display vertical refresh rates.

4. (Previously presented) The display controller of claim 7 where the failsafe circuit comprises:

a flip-flop to generate a first signal responsive to the input vertical refresh rate;

an inverter to generate a second signal by inverting the first signal, the second signal being provided to the flip-flop;

a logic gate to generate the internal vertical refresh rate by logically manipulating the first signal and the input vertical refresh rate;

a multiplexer to provide the internal vertical refresh rate to an output terminal responsive to the failsafe enable signal.

5. (Previously presented) The display controller of claim 7 where the internal vertical refresh rate is half the input vertical refresh rate.

6. (Previously presented) The display controller of claim 7 where there exists two input vertical refresh rate pulses for every one internal vertical refresh rate pulse.

7. (Previously presented) A display controller adapted to display image data received at an input vertical refresh rate on a display having a display vertical refresh rate, comprising:

a failsafe enable circuit to generate a failsafe enable signal responsive to the input vertical refresh rate; and

a failsafe circuit to generate an internal vertical refresh rate responsive to the failsafe enable signal, the internal vertical refresh rate being a predetermined fraction of the input vertical refresh rate;

where the system controller operates responsive to one of a plurality of modes comprising:

a display first mode where a first frame of the image data is displayed on the display while other frames are discarded in a single output frame;

a display last mode where a last frame of the image data is displayed on the display while other frames are discarded in the single output frame;

a display all mode where all frames of the image data are displayed on the single output frame.

8. (Previously presented) The display controller of claim 7 comprising:

a memory to store portions of the image data; and

an image scalar to resize the image data stored in the memory.

9. (Canceled)

10. (Previously presented) The system of claim 26 where the failsafe circuit comprises:

a flip-flop to generate a first signal responsive to the input vertical refresh rate;

an inverter to invert the first signal;

a logic gate to generate the internal vertical refresh rate by logically manipulating the first signal and the input vertical refresh rate; and

a multiplexer to select the internal vertical refresh rate responsive to the enable signal.

11. (Previously presented) The system of claim 26 where the display displays the image signals at the internal vertical refresh rate.

12. (Previously presented) The system of claim 26 where the internal vertical refresh rate is less than the display vertical refresh rate such that the image signals displayed on the display occupy less than a full vertical length of the display.

13. (Previously presented) The system of claim 26 where the internal vertical refresh rate is half the input vertical refresh rate.

14. (Previously presented) A system for visually displaying digital images, comprising:

image signals provided to the system one frame at a time, the image signals having an input vertical refresh rate;

a display capable to display the image signals having a display vertical refresh rate;

a failsafe enable to identify when the input vertical refresh rate exceeds the display vertical refresh rate and generate an enable signal responsive to the identification;

a failsafe circuit to generate an internal vertical refresh rate a predetermined fraction of the input vertical refresh rate responsive to the enable signal;

where the internal vertical refresh rate is half the input vertical refresh rate;

where the failsafe circuit comprises:

a display first mode where a first input frame is displayed on a single output frame while a second input frame is discarded;

a display last mode where the second input frame is displayed on the single output frame while the first input frame is discarded; and

display both mode where both the first and second input frames are displayed on the single output frame.

15. (Canceled)

16. (Previously presented) The failsafe circuit of claim 18 where the factor is half.

17. (Previously presented) The failsafe circuit of claim 18 where the failsafe circuit includes a mode circuit to generate a mode signal responsive to user input indicative of one of a plurality of modes.

18. (Currently amended) A failsafe circuit comprising:

a flip-flop adapted to generate a first signal responsive to an input vertical refresh rate;

an inverter adapted to invert the first signal;

a logic gate adapted to generate an internal vertical refresh rate by logically manipulating the first signal and the input vertical refresh rate, the internal vertical refresh rate being a factor of the input vertical refresh rate;

a multiplexer adapted to select the internal vertical refresh rate responsive to the enable signal; and

a mode circuit adapted to generate a mode signal responsive to user input indicative of one of a plurality of modes;

wherein the plurality of modes, comprises:

a display first mode wherein a first frame is received during a predetermined interval is displayed on a single output frame while other frames received during the predetermined time interval are discarded;

a display last mode wherein a last frame received during a predetermined time interval is displayed on the single output frame while other frames received during the predetermined time interval are discarded; and

a display all mode wherein all frames received during the predetermined time interval are displayed on the single output frame.

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Previously presented) A system for visually displaying digital images, comprising:

a display to display image signals having a display vertical refresh rate;

a failsafe enable to identify when the input vertical refresh rate exceeds the display vertical refresh rate and generate an enable signal responsive to the identification;

a failsafe circuit to generate an internal vertical refresh rate a predetermined fraction of the input vertical refresh rate responsive to the enable signal;

where the failsafe circuit operates in at least one of:

a display first mode where a first input frame is displayed on a single output frame while a second input frame is discarded;

a display last mode where the second input frame is displayed on the single output frame while the first input frame is discarded; or

display both mode where both the first and second input frames are displayed on the single output frame.